

ABSTRACT

A memory device that is comprised of a dynamic random access memory (DRAM) capacitor and a nitride read only memory (NROM) transistor. The memory device provides multiple modes of operation including a DRAM mode using the capacitor and a non-volatile random access memory mode using the NROM transistor. The device is comprised of two source/drain regions between which a gate insulator layer is formed. A control gate, coupled to a word line, is formed on top of the gate insulator. The DRAM capacitor is coupled to one of the source/drain regions while the second source/drain region is coupled to a bit line that is eventually coupled to a sense amplifier for reading the state or states of the memory device.